

# Computer Memory Test Labs Final Report

<u>MOTHERBOARD</u>	<u>MANUFACTURER</u>	<u>CHIPSET</u>	<u>TEST NUMBER</u>	<u>TEST STATUS</u>
D865PERL	Intel	Intel 865PE	008375	PASSED

### MODULE INFORMATION

Manufacturer Name: **Buffalo**  
 Part #: **DD333-1G/MD**  
 MB: **1GB**  
 Config: **128M x 64**  
 DRAM: **Micron**  
 DRAM Part #: **MT46V64M8TG(P)-6T rev D**  
 PCB Part: **UE0532-AA**  
 PCB\_layer\_count: **6 Layer**  
 Module Info: **Unbuffered      Non-ECC      333Mhz      DDR DIMM**  
 Cas Latency: **2.5**  
 Assembly Type: **Single Board/Non Stacked**

### SYSTEM INFORMATION

### TESTING DETAILS

#### MINIMUM SYSTEM INFORMATION

Minimum System: D865PERL      05-53  
 Board Revision: C27648-200  
 Post Memory Count: 1024  
 Processor Code: P4 2.53Ghz 533Mhz  
 Bios at time of test: RL86510A.86A.066.P11  
 MCFT Memory Count: 1023

#### MAXIMUM SYSTEM INFORMATION

Maximum System: D865PERL      05-53  
 Board Revision: C27648-200  
 Post Memory Count: 3808  
 Processor Code: P4 2.53Ghz 533Mhz  
 Bios at time of test: RL86510A.86A.066.P11  
 MCFT Memory Count: 3807

55°C Temperature: Standard Voltage  
 Start Date: 12/16/2004  
 Stop Date: 12/17/2004  
 Insertion Test: Pass  
 SPD Check: Pass  
 MCFT Min: Pass  
 MCFT Max: Pass  
 S3 Test: Pass  
 Power Cycle Test: Pass  
 Power Cycle Time: 38  
 OS: Windows  
 Service Pack: NA  
 Test Version: MCFT 1.4a

### VENDOR CONTACT INFORMATION

Contact: Tim Juarez      Contact Phone:      Purchase Order #:

Test Traveler Notes:

CMTL USE ONLY:

Verified by:

Emailed by:

Test Technician: Sonni Nguyen

In the event of a module failure, CMTL is not required to provide root cause analysis. Accuracy of testing is restricted to the above mentioned module with specific DRAM, PCB and other components as listed and tested with the CMTL Memory Compatibility Functionality Test, Microsoft Advanced Server 2000®, Windows NT 4.0 Enterprise Edition®, Windows XP®, Windows 98 SE®, Dos 6.22®, MStRESS® (v x.x), XLINEAR® (v x.xx), FXLINEAR® (v x.xx), Patin® (v x.x), WinMTA® (v x.xx). (Voltage margining applied only to those systems that are applicable.)

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